What is Claimed is:

[c1] A fuse element formed on a semiconductor substrate, the substrate having a subset of integrated circuit elements thereon having a minimum normal design width which is smaller than the width of other integrated circuit elements on said substrate and that receive first and second power supply voltages, a conductive line formed on said substrate and having two end portions and a center portion of said minimum normal design width, and a link portion within said center portion and spaced from said end portions which has a sub-minimum width less than said minimum normal design width, wherein an application of said first and second power supply voltages across said end portions causes an electrical property of said fuse element to undergo a detectable change.

[c2] The fuse element and semiconductor substrate of claim 1, wherein the conductive line includes a silicide thereon.

[c3] The fuse element and semiconductor substrate of claim 2, wherein the changed electrical property is resistance of the conductive line.

[c4] The fuse element and semiconductor substrate of claim 1, wherein the conductive line comprises a silicided gate of an FET, having an underlying doped poly.

[c5] The fuse element and semiconductor substrate of claim 4, wherein the changed electrical property is resistance of the FET.

[c6] The fuse element and semiconductor substrate of claim 4, wherein the changed electrical property is a threshold voltage of the FET.

[c7] The fuse element and semiconductor substrate of claim 1, wherein the spacing between the center portion and the end portions is sufficient to prevent the end portions from serving as a heat sink to increase the amount of joule heating required to change the electrical property.

[c8] The fuse element and semiconductor substrate of claim 7, wherein the minimum normal design width approximately 0.13 microns, and the sub-minimum width is approximately 0.5 microns.

[c9] The fuse element and semiconductor substrate of claim 7, wherein the link portion is

approximately at the center of the center portion.

[c10] The fuse element and semiconductor substrate of claim 1, including a polysilicon E-Fuse which includes a narrow sub-minimum width polysilicon line to provide increased self heating during programming when a current is passed through the E-Fuse.

[c11] The fuse element and semiconductor substrate of claim 10, wherein the polysilicon E-fuse uses a shorted/open line to distinguish a programmed/unprogrammed E-Fuse.

[c12] The fuse element and semiconductor substrate of claim 10, wherein the polysilicon E-fuse uses a change in resistance to distinguish a programmed/unprogrammed E-Fuse.

[c13] The fuse element and semiconductor substrate of claim 1, including a work function altered MOSFET selfâ€"aligned E-Fuse which includes a narrow sub-minimum width polysilicon line to provide increased self heating during programming when a current is passed through the E-Fuse, which drives dopant from the narrow polysilicon line, self-aligning an active area to this region, which causes a significant decrease in current through the MOSFET E-Fuse, to distinguish an unprogrammed/programmed E-Fuse.

[c14] The fuse element and semiconductor substrate of claim 1, including a MOSFET wherein increasing the field in a local region of a channel of the MOSFET causes a low voltage snapback in the MOSFET, which significantly increases the current flow through the MOSFET, such that the device is fused from drain to source, enabling the device to be used as an anti-E-Fuse.

[c15] The fuse element and semiconductor substrate of claim 1, including a MOSFET wherein increasing the field in a local region of a channel of the MOSFET causes allow voltage snapback in the MOSFET, and which includes a narrow sub-minimum width polysilicon line which allows for self-aligning source and drain contacts in a snapback region which provide a design for handling high program currents.

[c16] A mask used to form a sub-minimum image, comprising a first minimum size feature, and a second minimum size feature that is offset and spaced from said first minimum size feature.

[c17] A process of forming a sub-minimum size feature on a substrate, comprising:
forming a photosensitive polymer on the substrate;

exposing said photosensitive polymer to actinic radiation through a mask having a first minimum size feature and a second minimum size feature that is offset and spaced from said first minimum size feature; and

developing said polymer such that said sub-minimum size feature is defined by a portion of the mask between said minimum size features.

[c18] The process of claim 11, including forming an FET link as the sub-minimum feature.